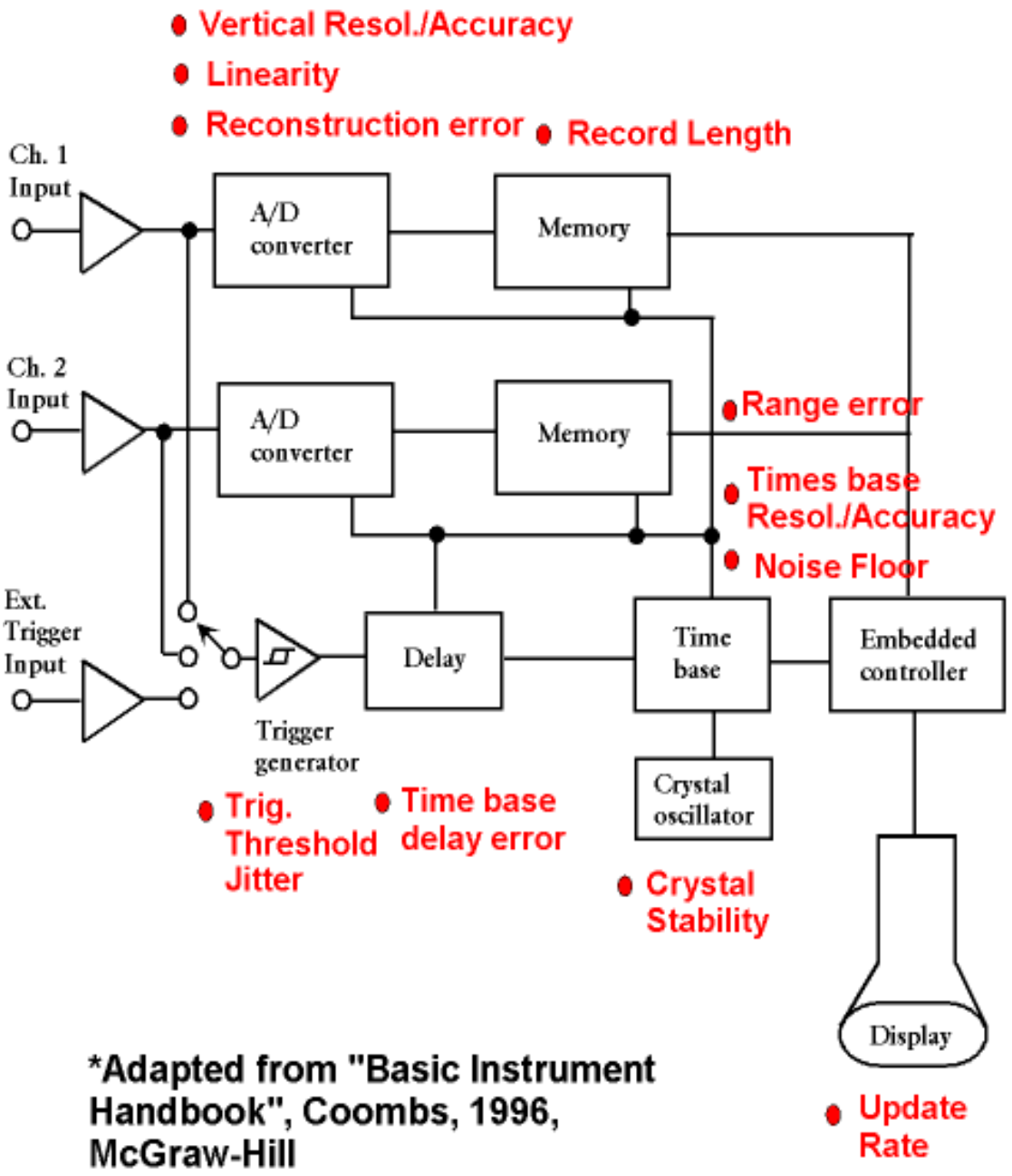
APPENDIX A

AVAILABLE EQUIPMENT

- DSO – Digital Sampling Oscilloscope (one-shot/repetitive)
- TIA – Time Interval Analyzer (MDA)
- BERT – Bit Error Rate Tester
- DTS-2070/2075 – Digital Time System
- Spectrum Analyzer
- ATE
- Custom

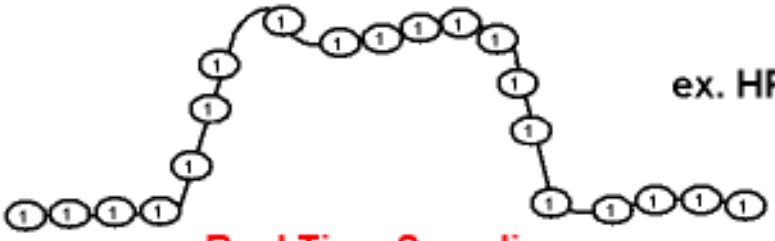
General Purpose Digital Sampling Oscilloscope

(key performance specifications)*



*Adapted from "Basic Instrument Handbook", Coombs, 1996, McGraw-Hill

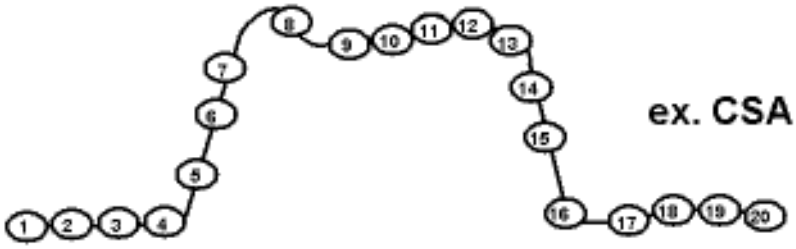
DSO Sampling Modes*



ex. HP54720D

Real Time Sampling

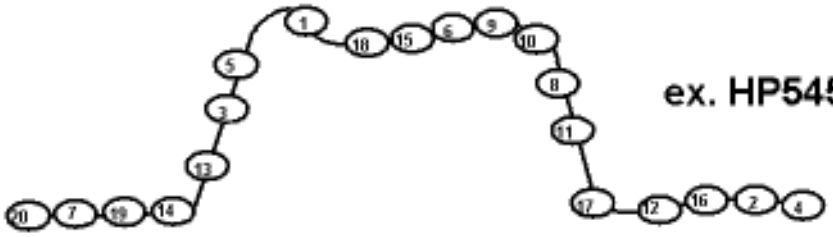
This sampling method captures entire waveform upon a single trigger event.



ex. CSA 803A

Sequential Repetitive Sampling

This sampling method acquires a new sample at a certain time interval after the trigger. Instrument increases this time delay by a fixed amount after each sample.



ex. HP54520C

Random Repetitve Sampling

Similar to Sequential Sampling except that the time difference between the trigger point and the sample point is random. Sampling is done constantly not waiting for a trigger event.

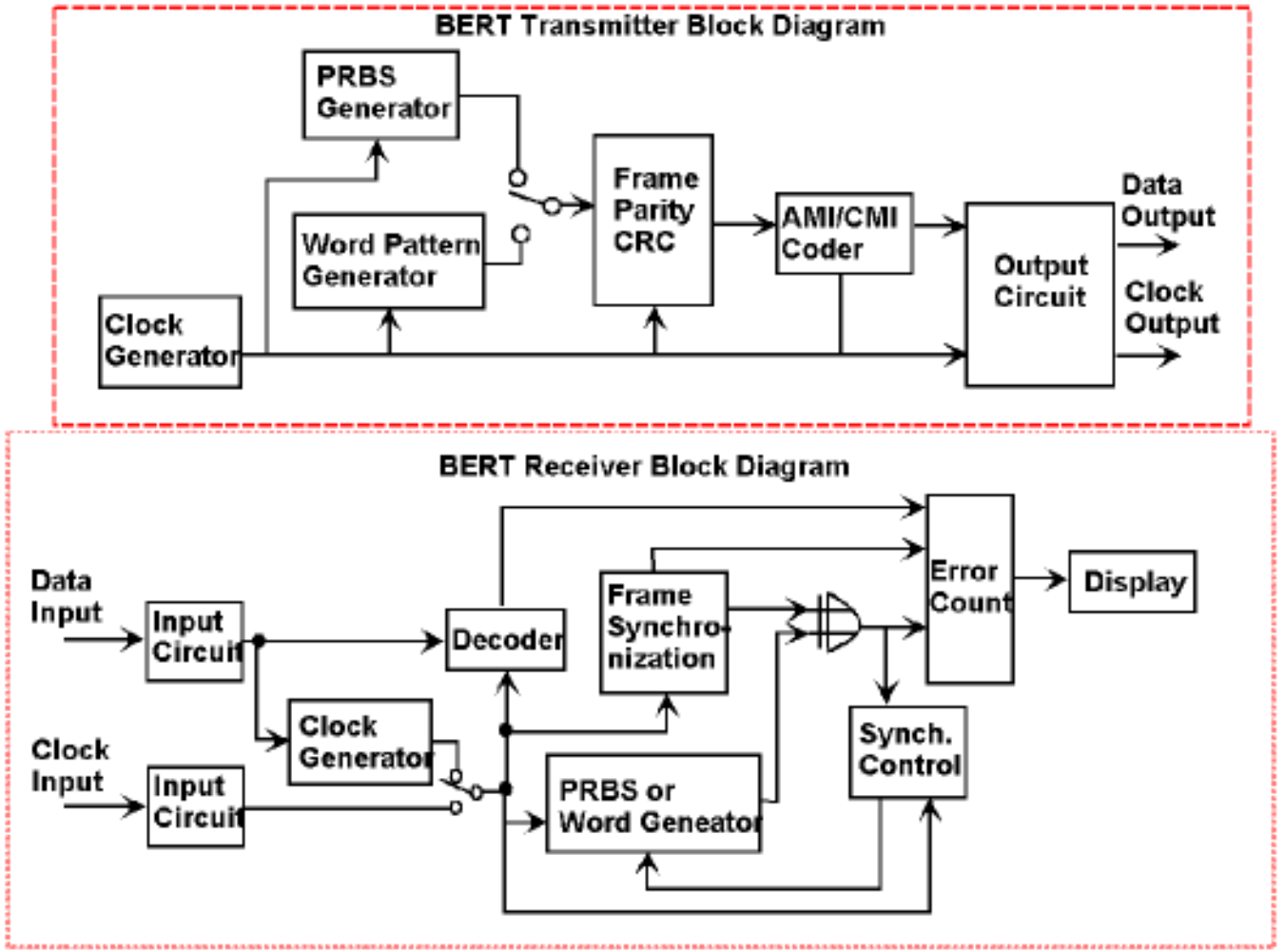
○ =represents data for a given trigger event

*Adapted from "A simple analysis helps to clarify a DSO's performance specs", EDN, Feb. 16, 1989

DSO's (Advantages/Disadvantages)

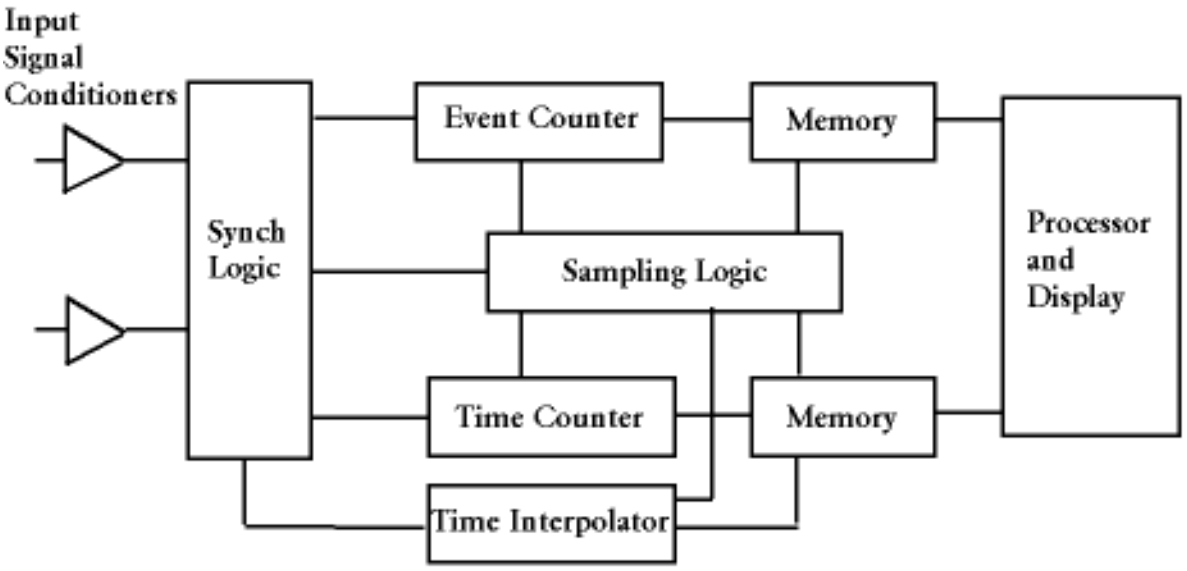
	Real Time Sampling	Random Repetitive Sampling	Sequential Repetitive Sampling
ADVANTAGES	One shot digitizing	Higher BW	Highest BW
		Cheaper A/D required	Cheaper A/D required
		Waveform viewing before trigger	
DISADVANTAGES	Lower BW	Trigger jitter concerns	Trigger jitter concerns
	BW is function of sampling rate BW = Fs/N (N from 2-4)	Require Sample and Hold circuit	Require Sample and Hold circuit
	Require reconstruction (digital filtering)	Not capable of single shot digitizing	Not capable of single shot digitizing
	May require BW limiting (Nyquist Criteria)		Cannot display trigger event without delay line

BERT Block Diagram*



*Adapted from "Basic Knowledge about Error Rate Measuring Instrument" Anritsu, 1992 Technical Note

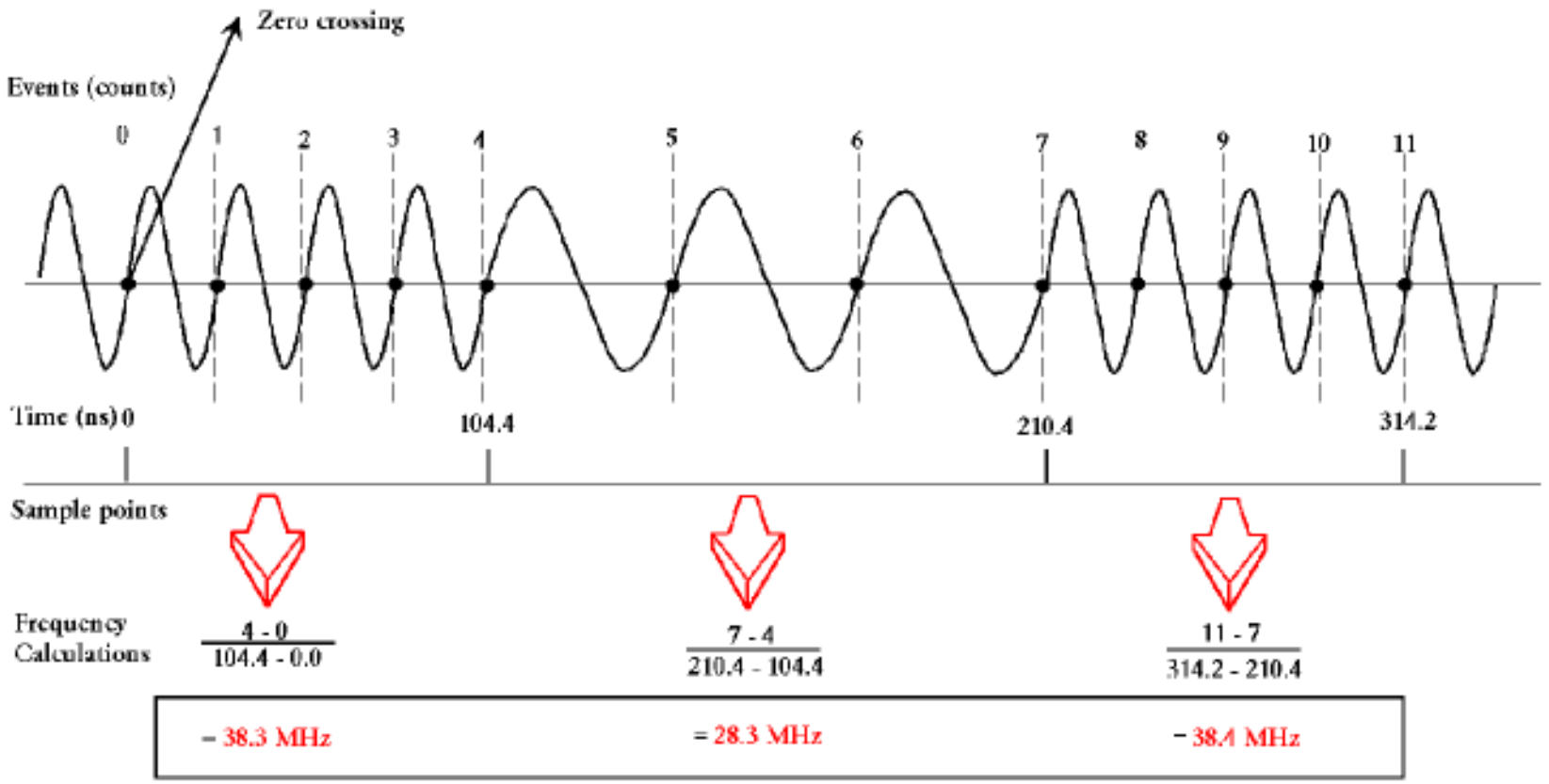
General TIA/MDA Block Diagram*



When sampling logic triggers a sample, the contents of the counters and interpolator is read into the next free memory location. The interpolator is then reset for the next sample point. Samples are taken until the specified number is reached and the memory is then read by the processor for calculations and display. Unlike a counter, the display is often graphic-based.

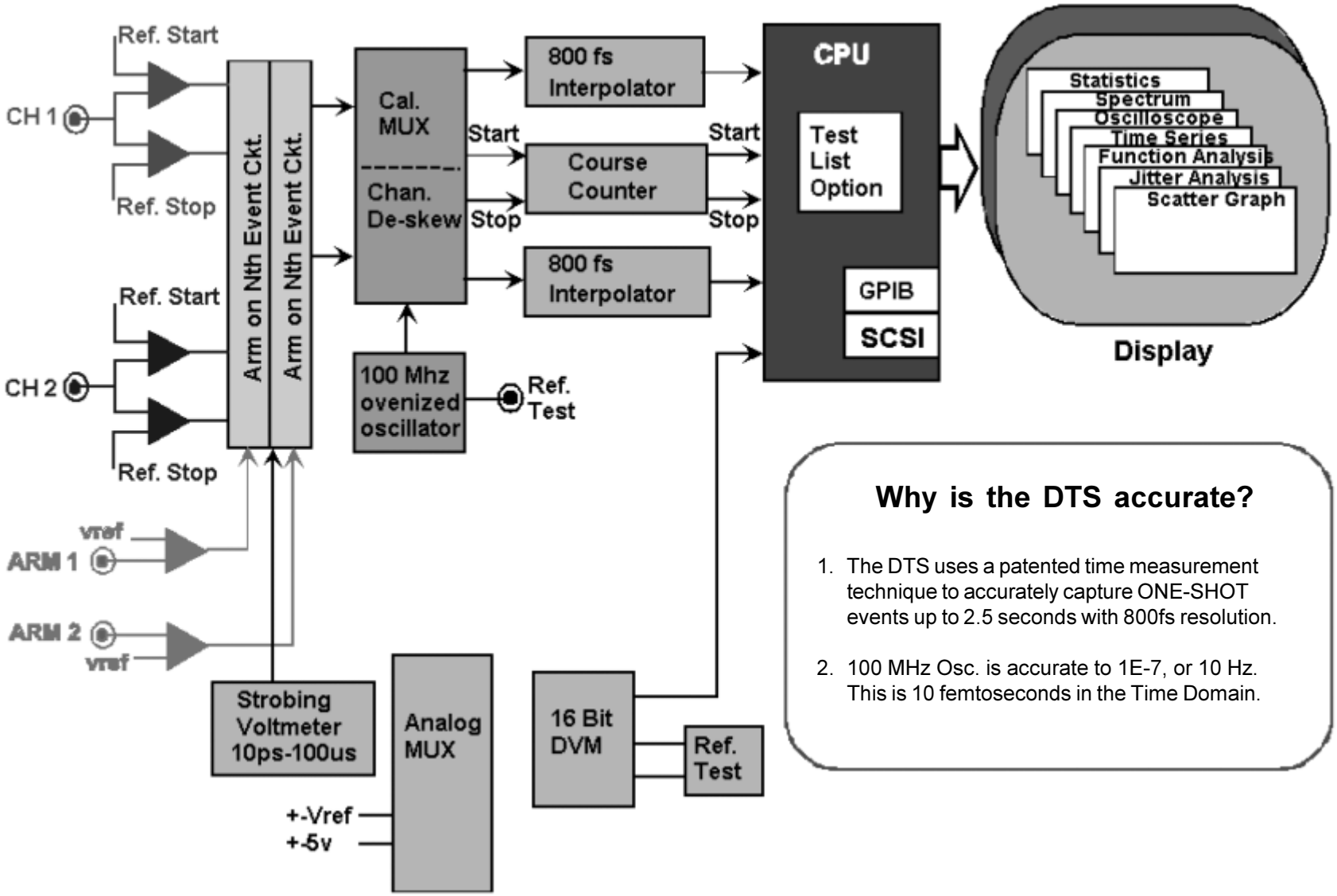
*Adapted from "Basic Instrument Handbook", Coombs, 1996, McGraw-Hill

Basic measurements made by a Time Interval Analyzer/Modulation Domain Analyzer*



*Adapted from "Basic Instrument Handbook", Coombs, 1996, McGraw-Hill

DTS 2070/2075 Block Diagram

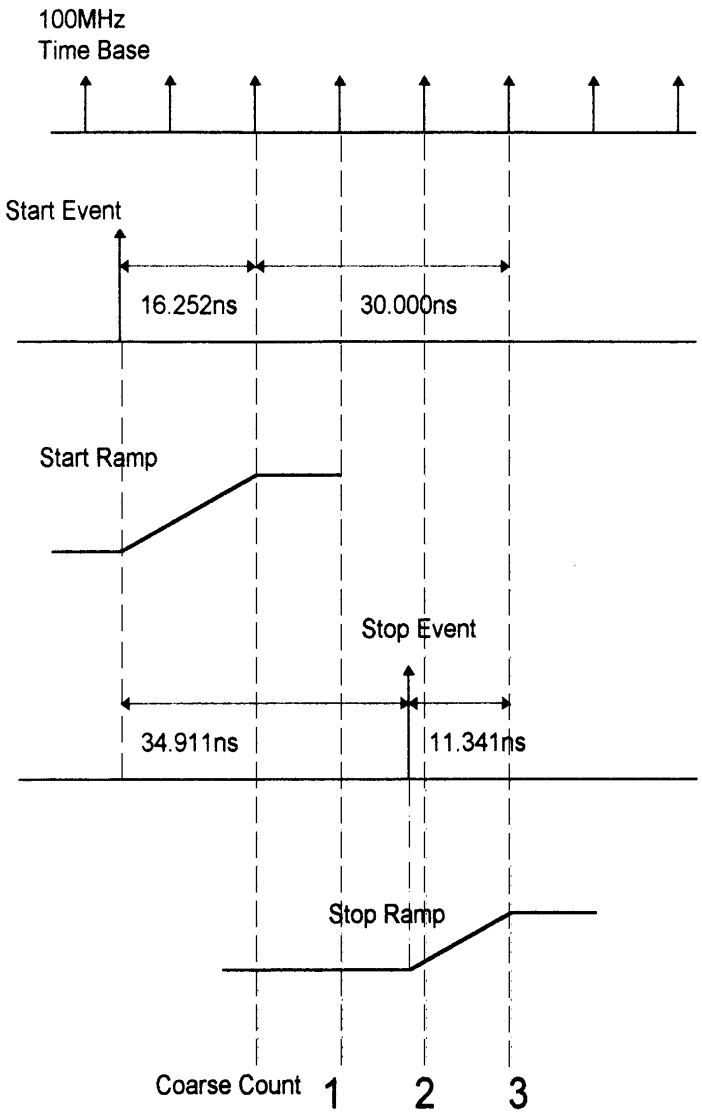


Why is the DTS accurate?

1. The DTS uses a patented time measurement technique to accurately capture ONE-SHOT events up to 2.5 seconds with 800fs resolution.

2. 100 MHz Osc. is accurate to 1E-7, or 10 Hz. This is 10 femtoseconds in the Time Domain.

DTS Time Interval Measurement Technique



Start Ramp Begins at Start Event and Ends at Second Time Base Edge After Start Event.

Stop Ramp Begins at Stop Event and Ends at Second Time Base Edge After Stop Event.

Height of Each Ramp is Digitized using a 14 Bit ADC

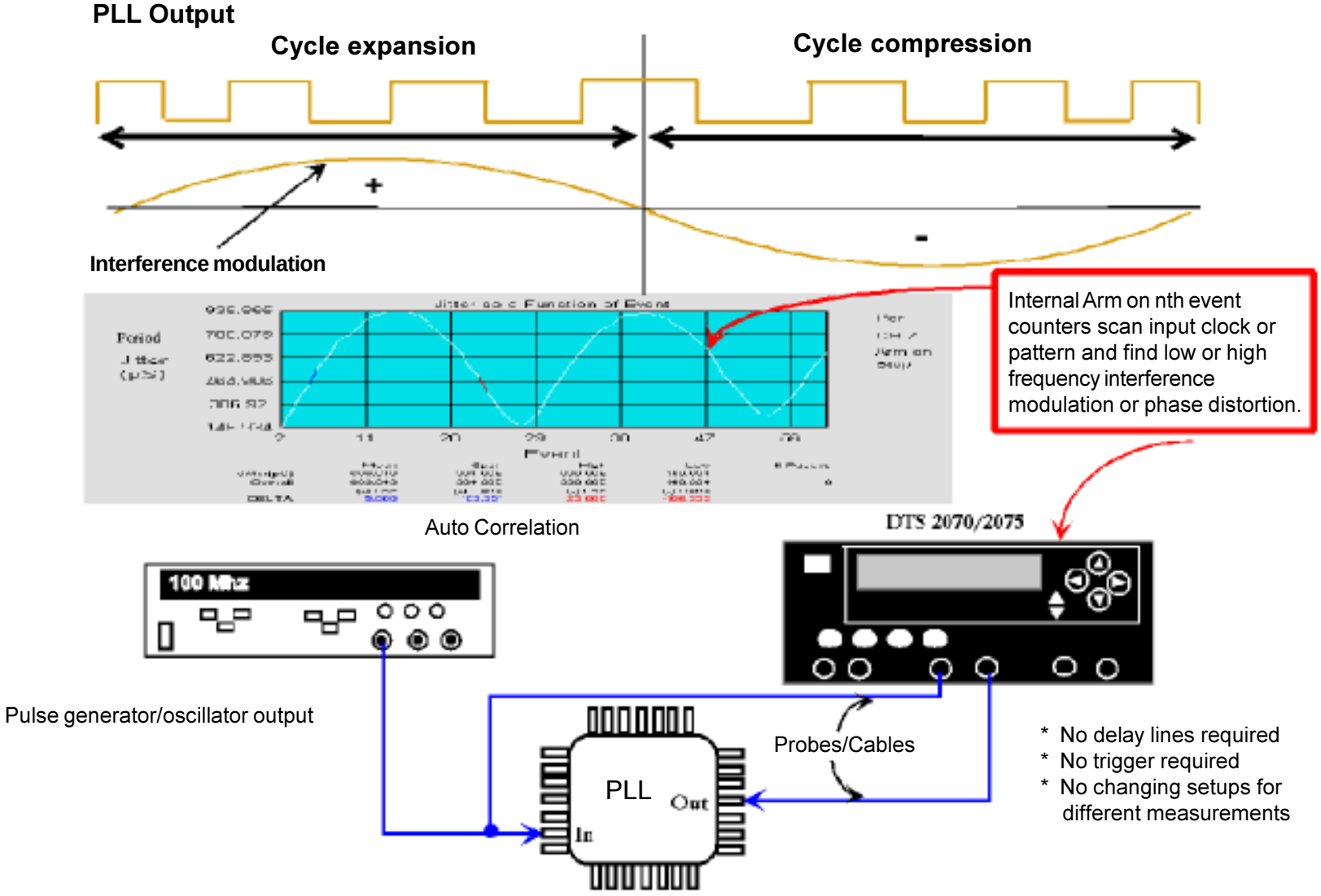
Coarse Counter Counts the Number of Time Base Periods Between Ends of Start and Stop Ramps.

$$N_{coarse\_count} * 10ns + T_{start\_ramp} - T_{stop\_ramp} = T_{measured\_interval}$$

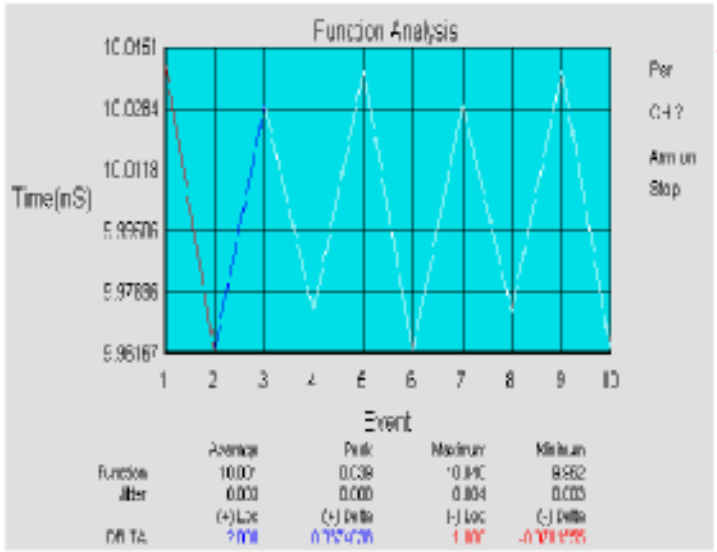
Example:

$$3 * 10.000ns + 16.252ns - 11.341ns = 34.911ns$$

Low Frequency Jitter Analysis (Modulation Domain)



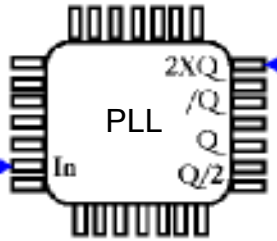
Synchronous Cycle to Cycle Jitter

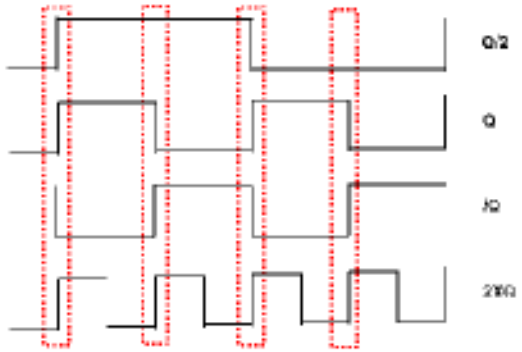


The outputs of the PLL have the following phase relationships. These relationships lead to 4 unique coincidental switching activities. These switching activities lead to 4 repetitive cycle-by-cycle period deviations.

Pulse generator/oscillator

ARM necessary to look at individual pulses in a train





Analysis Tools required to analyze various types of jitter

	Jitter Types				
Jitter Analysis Tools	**Synchronous mod./jitter**	**Asychronous mod./jitter**	**Cycle to cycle jitter (short cycle)**	**I/O Jitter**	**Long Term jitter (Wander)**
Histogram	x	x	x	x	
Freq. based Jitter Analysis (FFT)	x	x	x		
Time based Jitter Analysis (Mod. Domain)	x	x		x	
Function Analysis/Real Time	x		x		
Time Series/Scatter Graph	x	x			x
Waveform Capture	-	-	-	-	-

General Instrument Advantages/Disadvantages

	Jitter Analysis Tools and Features						
Instruments	Histogram	FFT	Jitter Analysis (Time Domain)	Function Analysis (Time/Freq.)	Speed	Waveform Capture	I/O Jitter Capability
DTS 2070/2075	Y	Y	Y	Y	Fast	Y	Y
TIA/MDA*	Y	?	?	?	Fast	N	N
Sampling Scopes*	Y	?	N	N	Slow	Y	Y
Real Time*	Y	?	?	?	Very Slow	Y	N
Digitizers							

*

Key Issues

- instrument noise floor
- f_{max} and bandwidth
- time/voltage resolution
- calibration methodology

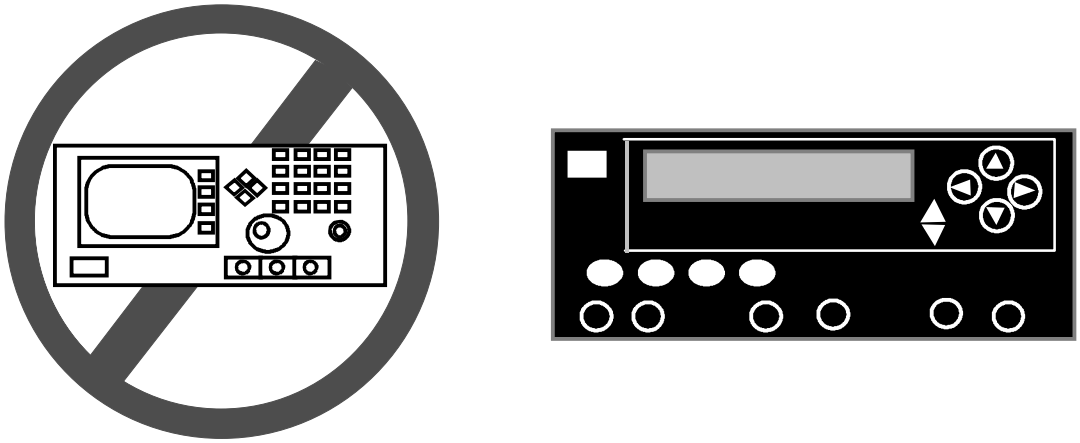
Main Issues for Accurate Jitter Analysis Instrument

- **Maximum usable frequency**
- **Input bandwidth**
- **Jitter noise floor**
- **Smallest one-shot resolution vs. linearity**
- **Correlated measurement record length**
- **Throughput**
- **Frequency/time correlation**

REASONS DTS CAN MEASURE JITTER MODULATION AND DSO CANNOT

CAN I MEASURE JITTER MODULATION??

DSO **DTS 2070/2075**



NO **YES**

- Jitter phase modulation induced onto a clock signal is in the **modulation domain** not the voltage vs. time domain. Modulation domain jitter is at or below the Nyquist frequency of the clock frequency.

- The Digital Sampling Oscilloscope (DSO) with its **trigger** based voltage vs. Time technique does not have the necessary triggering method or record length to capture enough relevant data for adequate determination of jitter in the **modulation domain,** even with using its FFT algorithms.

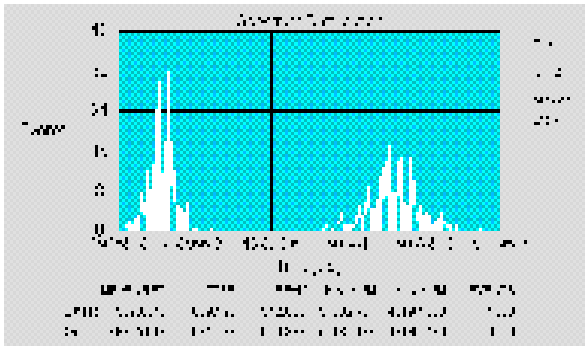
- The DTS 2070/2075 are designed to **directly** measure **modulation domain** information using a hardware and software implementation of a DSP technique called “Auto Correlation”.

UNIQUE PROPERTIES OF DTS 2070/2075

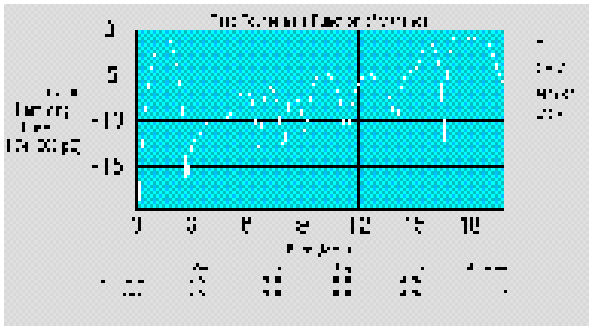
- **42 bits, one range, one-shot time measurement**
- **800fs timing resolution**
- **3ps noise floor**
- **Ability to measure jitter on 10 different pulse timing attributes (TPD++, TPD—, TPD+-, TPD-+, TT+, TT-, PW+, PW-, Period, Frequency); including True I/O jitter measurements.**
- **Arm on nth event (for low frequency modulation and FFT analysis and pattern dependency)**
- **Built in timing and linearity calibration**
- **Two channel De-skewing**
- **DC Calibration of Input Probe effect (if desired)**
- **Measuring events synchronously or asynchronously**
- **Extensive graphical analysis tool**
- **Interface to both popular PC and Unix environment**
- **Easy interface to ATE**

DTS 2070/2075 Measurement Techniques
Examples Of:

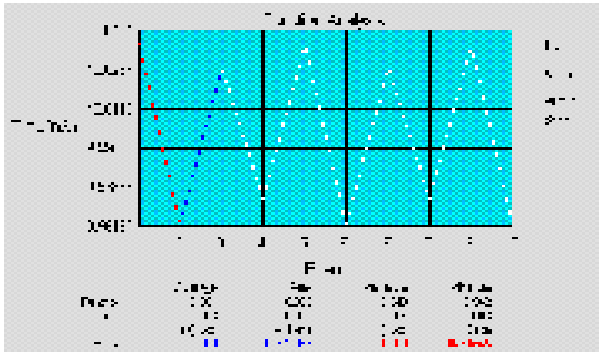
Jitter Histogram
(Threshold Spectrum Analysis)—short cycle



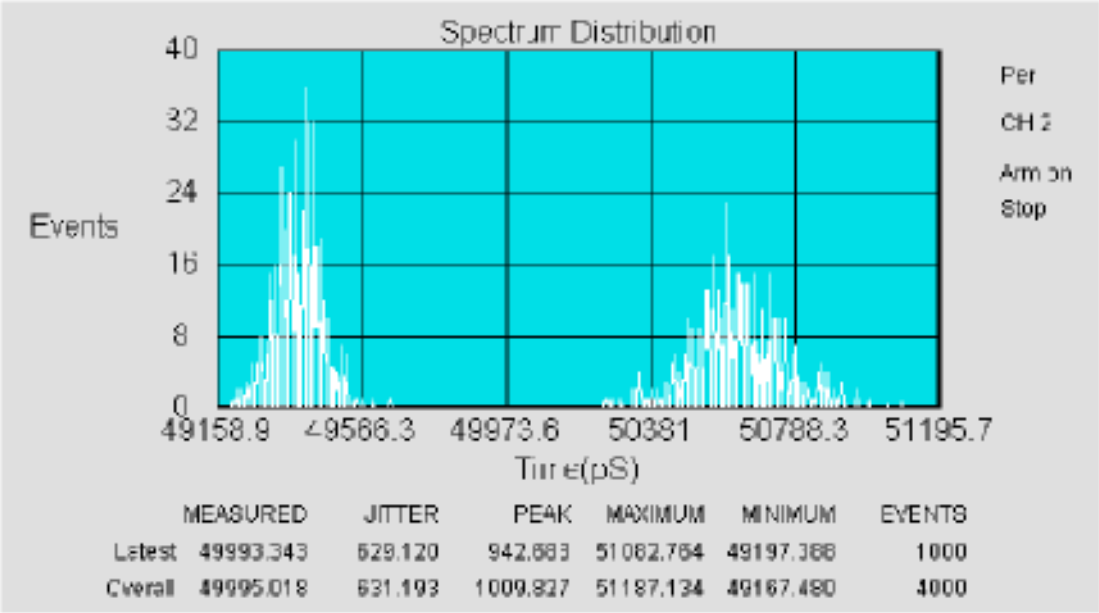
Asynchronous Jitter
(Jitter Analysis)—Modulation Domain



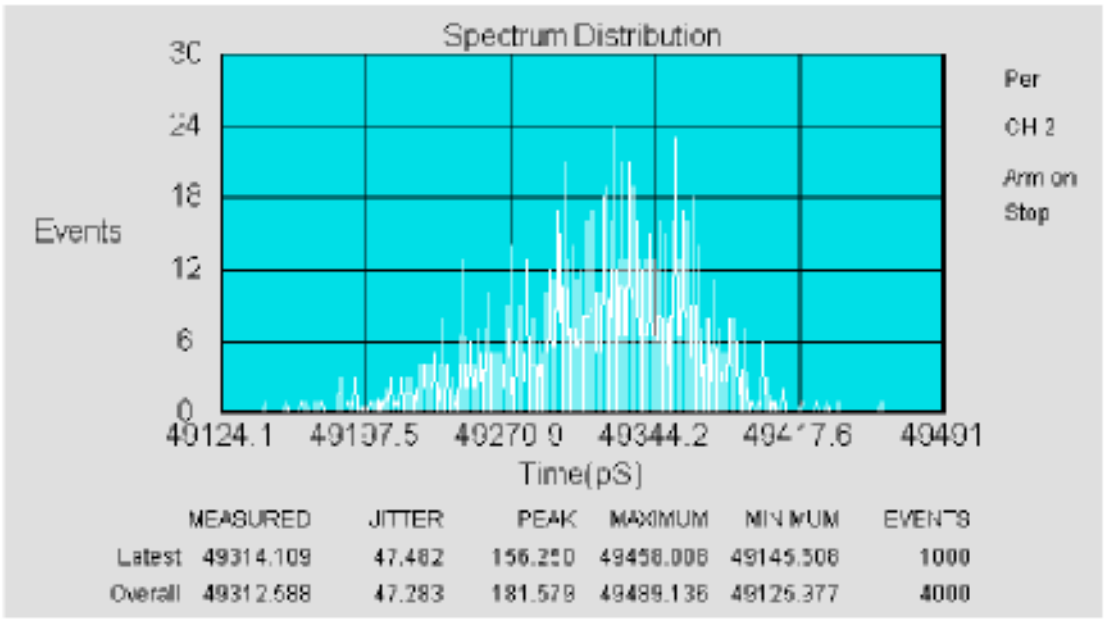
Synchronous Jitter
(Function Analysis)—cycle to cycle



Histogram (Spectrum Analysis)

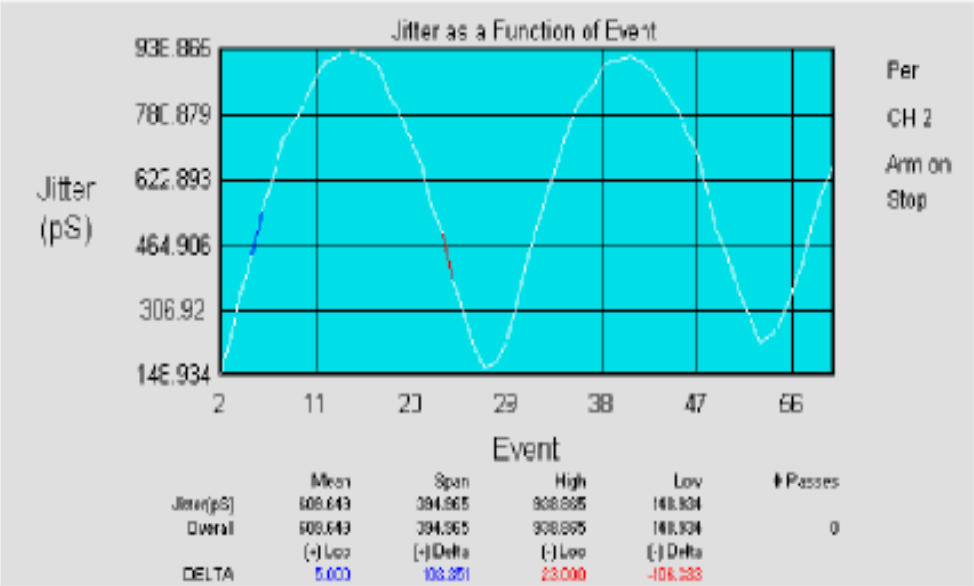


Plot is a period histogram of the 2XQ output of an off the shelf PLL. Input frequency is 10MHz; Output frequency is 20MHz, or 50ns period. Measurement is done automatically without external arming. Sample size = 1000.

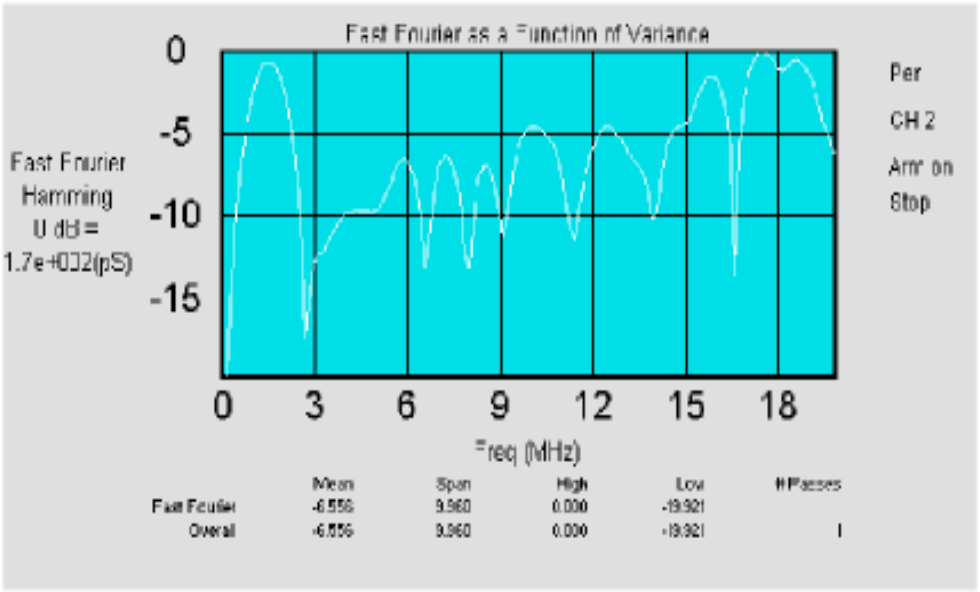


Details are the same as the first plot but external arming was used.

Asynchronous Jitter (Jitter Analysis and FFT)

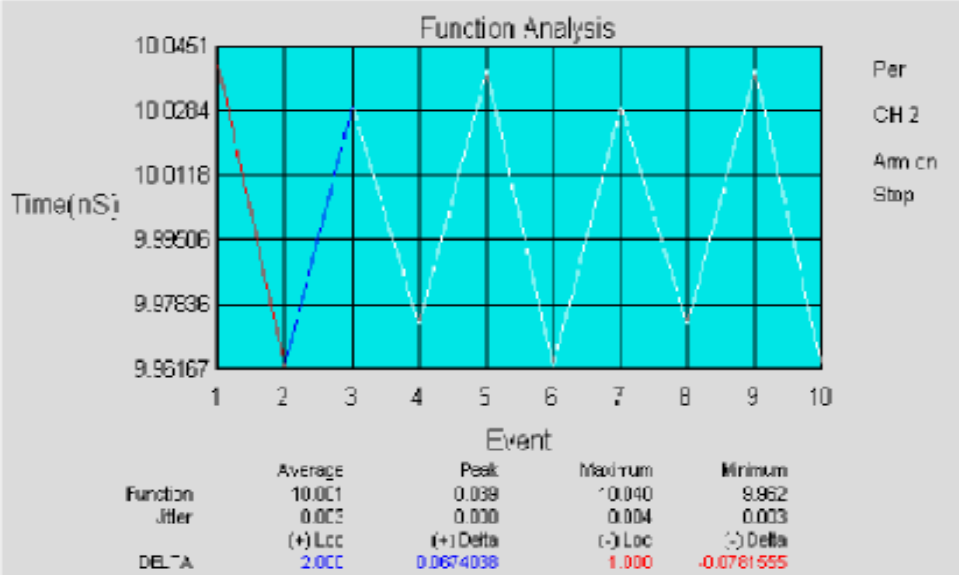


Plot shows jitter accumulation on the 2XQ output of an off-the-shelf PLL. Input frequency equals 20MHz; Output frequency is 40MHz. Plot shows jitter buildup over 28 consecutive cycles.



Plot shows an FFT analysis of the 2XQ output of the PLL with the same conditions used for Jitter Accumulation. Notice the FFT peak at 1.5MHz which corresponds to the modulation frequency calculated in Jitter Analysis (Modulation Domain).

Synchronous Jitter (Function Analysis)



Above is a period Function Analysis plot of the 2XQ output of an off-the-shelf PLL. Input frequency is 50MHz; output is 100MHz or 10ns period.

As can be seen, the period deviation pattern repeats every 4 cycles.